June 13, 2025

CONFERENCE WEBSITE: https://riscv.epcc.ed.ac.uk/community/workshops/isc25-workshop/

About the Conference

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CALL FOR PAPERS

International workshop on RISC-V for HPC (RISC-V HPC)

Held in conjunction with ISC25 on 13th June 2025

https://riscv.epcc.ed.ac.uk/community/workshops/isc25-workshop/

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Paper Deadline: 16th March 2025 (AoE)
Author Notification: 3rd April 2025
Camera ready papers: 16th May 2025

RISC-V is an open standard Instruction Set Architecture (ISA) which enables the royalty free development of CPUs and a common software ecosystem to be shared across them. Following this community driven ISA standard, a very diverse set of CPUs have been, and continue to be, developed which are suited to a range of workloads. Whilst RISC-V has become very popular already in some fields, and it is estimated over fifteen billion RISC-V cores have been shipped, to date it has yet to gain traction in HPC.

The goal of this workshop is to continue building the community of RISC-V in HPC, sharing the benefits of this technology with domain scientists, tool developers, and supercomputer operators. There are numerous potential advantages that RISC-V can provide to HPC and, assuming the significant rate of growth of this technology to date continues, as we progress further into the decade it is highly likely that RISC-V will become more relevant and widespread for HPC workloads. Furthermore, recent advances in RISC-V make it a more realistic proposition for HPC workloads than ever before.

The open and standardised nature of RISC-V means that the large, and growing community, can be involved in shaping the standard and tooling. This is important from two perspectives, firstly it is our

Important Dates

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opportunity in the HPC community to help shape the future of RISC-V to ensure that it is suitable for the next generation of supercomputers. Secondly, whilst there are a wide variety of RISC-V CPUs currently available, the standard nature of the tooling means that very often the same software ecosystem comprising the compiler, operating system, and libraries will run across these whilst requiring few changes.

This workshop aims to bring together those already looking to popularise RISC-V in the field of HPC with the supercomputing community at-large. By sharing benefits of the architecture, success stories, and techniques we hope to further popularise the technology and increase involvement by the community.

Call for papers and workshop topics

We invite submissions of high-quality, original research results and works-in-progress on RISC-V with a general connection to HPC. Topics of interest for this workshop include (but are not limited to):

* Example use-cases and case-studies that use RISC-V
* Lessons learnt from leveraging RISC-V in HPC
* Industry papers exploring the use of RISC-V
* The porting of codes to RISC-V
* Novel hardware and accelerators built upon RISC-V
* Tools and techniques to aid in the use of RISC-V for HPC
* Developments in HPC libraries to port them to RISC-V
* Enhancements to RISC-V to make the architecture more suited for HPC
* Compiler and runtime support for RISC-V
* The RISC-V ecosystem
* Future gazing how RISC-V might evolve the HPC community
* And anything else related to RISC-V and HPC!

Paper submission details

Authors are invited to submit unpublished, original work. Accepted papers will appear in the ISC post-conference workshop proceedings in the Springer Lecture Notes in Computer Science (LNCS) series and submitted versions available online for the workshop. Submissions are of original work between 6 and 12 pages are welcomed on work-in-progress, position papers, or mature work. The page count does not include references, an additional two pages to address reviewer comments.

All papers should be submitted via EasyChair (https://easychair.org/conferences/?conf=riscvhpc25) and there are more details on the workshop website at https://riscv.epcc.ed.ac.uk/community/workshops/isc25-workshop/

All papers should be formatted Springer single column LNCS style, with formatting information and template (https://www.springer.com/gp/computer-science/lncs/conference-proceedings-guidelines)

Organising committee
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* Nick Brown (EPCC at the University of Edinburgh)
* Daniele Gregori (E4 Computer Engineering)
* David Donofrio (Tactical Computing Laboratories)
* Teresa Cervero (BSC)
* Matt Turner (Samsung)

Programme committee
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* Oliver Perks (Rivos)
* John Leidel (Tactical Computing Labs)
* Maurice Jamieson (EPCC)
* Ruyman Reyes (Codeplay)
* Luis Plana (BSC)
* Luc Berger-Vergait (Sandia National Laboratories)
* Chris Taylor (Tactical Computing Labs)

TOPICS OF INTEREST 1 topics

Research papers are invited in, but not limited to, the following areas:

- Uncategorized